Claim 35 recites a pixel comprising, *inter alia*, "a reset region of a first conductivity type fabricated in said substrate and coupled to said charge collection region ... configured to apply a reset charge to said charge collection region in response to a pulsed reset signal applied to said reset region; a pulsed voltage source for providing said pulsed reset signal; and a capacitor, said capacitor having a first terminal in electrical communication with said pulsed voltage source and a second terminal in electrical communication with said reset region" (emphasis added). As described in the specification at paragraph [0005], the claimed invention allows the conventional reset transistor to be omitted. *See* FIGs. 7 and 9, reproduced below. Applicant respectfully submits that Zhao et al. and Koichi et al. do not teach or suggest these limitations.

Claim 42 recites a pixel comprising, *inter alia*, "a charge collection region provided in a substrate; a reset region provided in said substrate adjacent said charge collection region for periodically resetting a charge level of said charge collection region ...; a source follower transistor ...; a pulsed voltage source ...; and a capacitor in electrical communication with said pulsed voltage source, said reset region, and said source follower transistor for storing charge collected in said charge collection region" (emphasis added). As described in the specification at paragraph [0005], the claimed invention allows the conventional reset transistor to be omitted. *See* FIGs. 7 and 9, reproduced below. Applicant respectfully submits that Zhao et al. and Koichi et al. do not teach or suggest these limitations.